

Remarks

Applicants respectfully request reconsideration and allowance in view of the foregoing amendments and following remarks. In the Office Action, mailed November 30, 2006, the examiner rejected claims 21-43. By this amendment, claims 21-43 are cancelled without prejudice and claims 44-55 are newly added in this response. No new matter is entered.

Claims 44-49 are newly added without entering any new matters

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Claim 44 recites:

Claim 44 (New): A driving circuit for outputting a differential signal, comprising:
an output circuit for outputting the differential signal according to a first voltage and a second voltage;
15 a control signal generator, coupled to the output circuit, for generating the first voltage and the second voltage, comprising:
a current mirror, comprising:
a first transistor having a gate;
a reference current generator, coupled to the gate of the first transistor,
20 for providing a reference current; and
a second transistor having a gate coupled to the gate of the first transistor and the reference current generator;
a first conducting path, coupled to the gate of the first transistor, the gate of the second transistor and the reference current generator, for providing
25 the first voltage to the output circuit according to the voltage of the gates of the first and second transistors; and
a second voltage generator for generating the second voltage to the output circuit; and
a switching circuit, coupled between the output circuit and the control signal
30 generator, for controlling the coupling and decoupling relation between the output circuit and the control signal generator such that the differential signal representing logic high or logic low according to the coupling and decoupling

relation between the output circuit and the control signal generator.

Concerning the patentability of the newly added independent claim 44 with respect to the prior art Dillon (U.S. Patent No. 6,700,403), claim 44 is patentable over
5 Dillon because Dillon fails to teach or suggest a combination of the limitations recited in claim 44. As claims 45-49 are dependent upon claim 44, if claim 44 is found to be allowable, so to should the dependent claims.

Claims 50-55 are newly added without entering any new matters

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Claim 50 recites:

Claim 50 (New): A driving circuit for outputting a differential signal, comprising:
an output circuit for outputting the differential signal according to a first voltage
and a second voltage, comprising:

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a first transistor operating in response to the first voltage;

a second transistor, coupled to the first transistor, operating in response to
the second voltage;

a first node between the first transistor and the second transistor for
outputting a part of the differential signal;

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a third transistor operating in response to the first voltage;

a fourth transistor, coupled to the third transistor, operating in response to
the second voltage; and

a second node between the third transistor and the fourth transistor for
outputting the other part of the differential signal;

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a control signal generator, coupled to the output circuit, for generating the first
voltage and the second voltage, comprising:

a voltage generating circuit for generating the first voltage and the second
voltage;

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a first conducting path, coupled between the voltage generating circuit and
the first transistor, for providing the first voltage to the first transistor
according to a switching control;

a second conducting path, coupled between the voltage generating circuit

and the second transistor, for providing the second voltage to the second transistor according to the switching control;

a third conducting path, coupled between the voltage generating circuit and the third transistor, for providing the first voltage to the third transistor according to the switching control; and

5 a fourth conducting path, coupled between the voltage generating circuit and the fourth transistor, for providing the second voltage to the fourth transistor according to the switching control; and

a switching circuit, coupled between the output circuit and the control signal generator, for determining the switching control that controls the coupling and decoupling relation between the output circuit and the control signal generator such that the differential signal representing logic high or logic low according to the coupling and decoupling relation between the output circuit and the control signal generator, the switching circuit comprising:

10 a first switch coupled between the control signal generator and the first transistor, the on/off state of the first switch determining whether the first conducting path provides the first voltage to the first transistor;

a second switch coupled between the control signal generator and the second transistor, the on/off state of the second switch determining whether the second conducting path provides the second voltage to the second transistor;

20 a third switch coupled between the control signal generator and the third transistor, the on/off state of the third switch determining whether the third conducting path provides the first voltage to the third transistor; and

25 a fourth switch coupled between the control signal generator and the fourth transistor, the on/off state of the fourth switch determining whether the fourth conducting path provides the second voltage to the fourth transistor.

30 Concerning the patentability of the newly added independent claim 50 with respect to the prior art Dillon (U.S. Patent No. 6,700,403), claim 50 is patentable over Dillon because Dillon fails to teach or suggest a combination of the limitations recited

in claim 50. As claims 51-55 are dependent upon claim 50, if claim 50 is found to be allowable, so to should the dependent claims.

- 5 Since the aforementioned amendments and reasons have put all of the remaining claims into the state of allowance, reconsideration of the current application by the examiner is hereby respectfully requested.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

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